CLAIMS

What is claimed is:

1. A method for forming a semiconductor structure comprising the steps of:

providing a structure having at least one wire bond pad in contact with a metal line of an interconnect structure, said at least one wire bond pad having an exposed surface portion;

forming a metallic cap on at least the exposed upper surface portion of the wire bond pad, said metallic cap is resistant to alkaline attack; and

forming Ni/Au metallization on said metallic cap.

2. The method of Claim 1 wherein the metallic cap is formed on the exposed surface portion of the wire bond pad through an opening formed in an overlaying passivation stack.

3. The method of Claim 1 wherein the metallic cap is formed atop an entire surface of a metal layer and then the metallic cap and metal layer are selectively etched to form the metallic cap on at least the exposed upper surface portion of the wire bond pad.

4. The method of Claim 1 wherein the metal line is comprised of Cu.

5. The method of Claim 1 wherein said structure further includes a barrier and a lower passivation layer formed atop the interconnect structure.

6. The method of Claim 1 wherein the wire bond pad is comprised of Al or an aluminum alloy.

7. The method of Claim 1 wherein the Ni/Au pad metallization is formed by electroless deposition of Ni, immersion deposition of Au and electroless deposition of Au.

8. The method of Claim 1 wherein the metallic cap comprises TiN/Ti or TiN/Al.

9. The method of Claim 8 wherein the Al layer of the metallic cap is cleaned/pretreated prior to forming the Ni/Au metallization.

10. The method of Claim 8 wherein the Ti layer of the metallic cap is activated prior to forming the Ni/Au metallization.

11. The method of Claim 1 further comprising forming a barrier layer between at least the metal bond pad and the metal line.

12. The method of Claim 1 wherein said metal bond pad and said metal line are in contact through a via opening formed in a lower passivation layer that is located on said interconnect structure.

13. A semiconductor structure comprising:

an interconnect structure containing an upper interconnect level having one or more metal lines, each metal line having a wire bond pad located on a surface thereof;

a metallic cap that is resistant to alkaline attack on a surface of the wire bond pad; and

Ni/Au pad metallurgy atop said metallic cap, said Ni/Au pad metallurgy is in electrical contact with said wire bond pad through said metallic cap.

14. The structure of Claim 13 wherein the wire bond pad is comprised of Al or an Al stack.

15. The structure of Claim 13 wherein each metal line is comprised of Cu.

16. The structure of Claim 13 wherein each metal bond pad is in contact with a corresponding metal line through a via opening located in a lower passivation layer that is located on said interconnect structure.

17. The structure of Claim 13 further comprising passivation layers encapsulating said wire bond pad and Ni/Au pad metallurgy.

18. The structure of Claim 17 wherein said passivation layers includes a lower passivation layer and overlying final passivation layers, said overlying final passivation layers comprising an oxide layer, a nitride layer and a layer of polyimide or a layer of polysiloxane.

19. The structure of Claim 13 wherein the metallic cap comprises TiN/Ti, said Ti is activated Ti.

20. The structure of Claim 13 wherein the metallic cap comprises TiN/Al, said Al is cleaned/pretreated Al.